Arman Roohi

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Professional Experience

2024-present **Associate Professor**, Electrical and Computer Engineering, University of Illinois - Chicago, Chicago, IL, USA.

2024-current **Adjunct Assistant Professor**, School of Computing, University of Nebraska - Lincoln, Lincoln, NE, USA.

2020-2024 **Assistant Professor**, School of Computing, University of Nebraska - Lincoln, Lincoln, NE, USA.

2019-2020 **Postdoctoral Research Fellow**, Electrical and Computer Engineering, University of Texas at Austin, Austin, TX, USA.

2016-2019 **Graduate Research Assistant**, Electrical and Computer Engineering, University of Central Florida, Orlando, FL, USA.

Education

2015–2019 **Ph.D, Computer Engineering**, *University of Central Florida*, Orlando, FL, USA.

2009–2011 **M.Sc., Computer Architecture**, *Science and Research Branch, Azad University*, Tehran, Iran.

2003–2008 **B.Sc., Computer Engineering, Hardware**, *Shiraz University*, Shiraz, Iran.

Research Interests

- Energy Efficient and High-Performance Processing in-Memory Circuit, Architecture and Algorithm
- Batteryless Processing and Learning Architecture
- Brain-Inspired Computing, Neuromorphic Computing, Machine Learning Acceleration
- Secure Computation including Hardware Security and Security of Artificial Intelligence
- Reconfigurable and Adaptive Computer Architectures

Academic Awards and Honors

- **CAREER Award**, National Science Foundation, 2024.
- **Nebraska EPSCoR FIRST Award**, University of Nebraska-Lincoln, 2023.
- **Outstanding Teaching Award - Graduate Level**, School of Computing, University of Nebraska-Lincoln, 2023.
- **Fellow of the Research Development Fellows Program**, Office of Research and Economic Development, University of Nebraska-Lincoln, 2020.
- College of Graduate Studies Conference Presentation Fellowship, University of Central Florida, 2015 - 2018. ($2000)
- Student Government Association Individual Conference Presentation Fellowship, University of Central Florida, 2016 - 2018. ($2000)
- Student Government Association Registered Student Organization Conference Participation Fellowship, University of Central Florida, 2017 - 2019. ($14000)
- (C40) **Best Paper Award Candidate**: International Symposium on Low Power Electronics and Design (ISLPED) 2023.
- (C13) **Best Paper Award Candidate**: International Symposium on Quality Electronic Design (ISQED) 2019.
- (C12) **Best Paper Award Candidate**: ACM Great Lakes Symposium on VLSI (GLSVLSI) 2018.

- (J14) **Paper of the Month**: IEEE Transactions on Emerging Topics in Computing, including free download as sole paper highlighted on that IEEE TETC home webpage 2018.
- (C11) **Best Paper Award Candidate**: International Symposium on Quality Electronic Design (ISQED) 2018.
- (J11) **Paper of the Month**: IEEE Transactions on Computers, June 2016, with hosted companion video featured on IEEE Transactions webpage 2016.
- **Invention Disclosure**, UCF Office of Research and Commercialization, "A Parity-Preserving Reversible QCA Gate with Cascadable Resilience," April 15, 2015.
- Ph.D. Forum at DAC 2018 Scholarship, with acceptance rate around 30% ($1200).
- 2018 Frank Hubbard Engineering Endowed Scholarship for the 2018-2019 academic year ($1000).

Publications and Patents

LEGEND

(*) Corresponding Author

Underline: Ph.D./Master students mentored by Dr. Arman Roohi

Jx. (Journal publication numbering)

Cx. (Conference publication numbering)

❑ Journal Papers

J35 S. Tabrizchi, B. Reidy, D. Najafi, Sh. Angizi, R. Zand, and **A. Roohi***, "ViTSen: Bridging Vision Transformers and Edge Computing with Advanced In/Near-Sensor Processing," *IEEE Embedded Systems Letters (ESL)*, 2024.

J34 N. Taheri, S. Tabrizchi, and **A. Roohi***, "Intermittent-Aware Design Exploration of Systolic Array Using Various Non-Volatile Memory: A Comparative Study," *Micromachines*, 2024.

J33 D. Najafi, M. Morsali, R. Zhou, **A. Roohi**, A. Marshall, D. Misra, and Sh. Angizi*, "Enabling Normally-Off In Situ Computing With a Magneto-Electric FET-Based SRAM Design," *IEEE Transactions on Electron Devices*, 71, no. 4, 2742-2748, 2024.

J32 **A. Roohi***, S. Tabrizchi, M. Morsali, D. Pan, and Sh. Angizi, "PiPSim: A Behavior-Level Modeling Tool for CNN Processing-in-Pixel Accelerators," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2023.

J31 Sh. Angizi*, S. Tabrizchi, D. Pan, and **A. Roohi***, "PISA: A Non-Volatile Processing-In-Sensor Accelerator for Imaging Systems," *IEEE Transactions on Emerging Topics in Computing*, 2023.

J30 M. Morsali, S. Tabrizchi, **A. Roohi** , and Sh. Angizi*, "Design and Evaluation of a Near-Sensor Magneto-Electric FET-based Event Detector," *IEEE Transactions on Electron Devices*, 2023.

J29 Sh. Angizi*, M. Morsali, S. Tabrizchi, and **A. Roohi***, "A Near-Sensor Processing Accelerator for Approximate Local Binary Pattern Networks," *IEEE Transactions on Emerging Topics in Computing*, 2023.

J28 S. Tabrizchi, A. Nezhadi, Sh. Angizi, and **A. Roohi***, "AppCiP: Energy-Efficient Approximate Convolution-in-Pixel Scheme for Neural Network Acceleration," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 2023.

J27 R. Zhou, S. Tabrizchi, **A. Roohi**, and Sh. Angizi*, "LT-PIM: An LUT-based Processing-in-DRAM Architecture with RowHammer Self-Tracking," *IEEE Computer Architecture Letters*, 2022.

J26 S. Tabrizchi, Sh. Angizi, and **A. Roohi***, "Ocelli: Efficient Processing-in-Pixel Array Enabling Edge Inference of Ternary Neural Networks," *Journal of Low Power Electronics and Applications*, 2022.

J25 N. Khoshavi*, M. Maghsoudloo, **A. Roohi**, S. Sargolzaei, and B. Yu, "HARDeNN: Hardware-assisted Attack-resilient Deep Neural Network Architectures," *Microprocessors & Microsystems*, 2022.

J24 M. Abedin, **A. Roohi**[*], M. Liehr, N. Cady, and Sh. Angizi[*], "MR-PIPA: An Integrated Multi-level RRAM (HfO_x) based Processing-In-Pixel Accelerator," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, 2022.**(Featured Paper)**

J23 M. Alali[*], **A. Roohi**[*], Sh. Angizi, and J. S. Deogun, "Enabling Intelligent IoTs for Histopathology Image Analysis Using Convolutional Neural Networks," *Micromachines*, 13, no. 8, 2022.

J22 **A. Roohi**[*], Sh. Angizi, Sh. Sheikhfaal, D. Fan, and R. F. DeMara, "ApGAN: Approximate GAN for Robust Low-Energy Learning from Imprecise Components," *IEEE Transactions on Computers*, October 2019.

J21 **A. Roohi**[*], and R. F. DeMara, "PARC: A Novel Design Methodology for Power Analysis Resilient Circuits Using Spintronics," *IEEE Transactions on Nanotechnology*, August 2019.

J20 **A. Roohi**[*], and R. F. DeMara, "NV-Clustering: Normally-Off Computing Using Non-Volatile Datapaths," *IEEE Transactions on Computers*, vol. 67, no. 7, pp. 949-959, July 2018.

J19 R. Zand[*], **A. Roohi**, and R. F. DeMara, "Energy-Efficient and Process-Variation-Resilient Write Circuit Schemes for Spin Hall Effect MRAM Device," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 9, pp. 2394-2401, Sept. 2017.

J18 **A. Roohi**[*], R. Zand, D. Fan, and R. F. DeMara, "Voltage-based Concatenatable Full Adder using Spin Hall Effect Switching," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 36, no. 12, pp. 2134-2138, Dec. 2017.

J17 M. K.Krishna, **A. Roohi**, R. Zand, D. Fan, and R. F. DeMara[*], "Heterogeneous Energy-Sparing Reconfigurable Logic: Spin-based Storage and CNFET-based Multiplexing," *IET Circuits, Devices & Systems*, vol. 11, no. 3, pp. 274-279, 5 2017.

J16 R. Zand, **A. Roohi**, D. Fan, and R. F. DeMara[*], "Energy-Efficient Nonvolatile Reconfigurable Logic using Spin Hall Effect-based Lookup Tables," *IEEE Transactions on Nanotechnology*, vol. 16, no. 1, pp. 32-43, Jan. 2017.

J15 A.M. Chabi, **A. Roohi**, H. Khademolhosseini, Sh. Sheikhfaal, Sh. Angizi, K. Navi, and R. F. DeMara[*], Towards Ultra-efficient QCA Reversible Circuits," *Microprocessors and Microsystems*, Volume 49, Pages 127-138, 2017.

J14 **A. Roohi**[*], R. Zand, Sh. Angizi, and R. F. DeMara, "A Parity-Preserving Reversible QCA Gate with Self-Checking Cascadable Resiliency," *IEEE Transactions on Emerging Topics in Computing*, Special Issue on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, vol. 6, no. 4, pp. 450-459, 2016. **(December 2018 Featured Paper, paper of the month)**

J13 **A. Roohi**[*], R. Zand, and R. F. DeMara, "A Tunable Majority Gate based Full Adder using Current-Induced Domain Wall Nanomagnets," *IEEE Transactions on Magnetics* 52 (8), 2016.

J12 R. Zand, **A. Roohi**, S. Salehi, and R. F. DeMara[*], "Scalable Adaptive Spintronic Reconfigurable Logic using Area-Matched MTJ Design," *IEEE Transactions on Circuits and Systems II: Express Briefs* 63 (7), 678 - 682, 2016.

J11 H. Shabani, **A. Roohi**, A. Reza, M. Reshadi, N. Bagherzadeh, and R. F. DeMara[*], "Loss-Aware Switch Design and Non-Blocking Detection Algorithm for Intra-Chip Scale Photonic Interconnection Networks," *IEEE Transactions on Computers*, 65 (6), 1789-1801, 2016. **(June 2016 Featured Paper, paper of the month)**

J10 **A. Roohi**[*], H. Thapliyal, and R. F. DeMara, "Wire Crossing Constrained QCA Circuit Design using Bilayer Logic Decomposition," *IET Electronics Letters*, Vol 51, No. 21, P. 1677, 2015.

J9 Sh. Angizi[*], S. Sayedsalehi, **A. Roohi**, N. Bagherzadeh, K. Navi, "Design and verification of new n-bit quantum-dot synchronous counters using majority function-based JK flip-flops," *Journal of Circuits, Systems and Computers*, Vol 24, No. 10, P. 1550153, 2015.

J8 **A. Roohi**[*], R. F. DeMara, and N. Khoshavi, ''Design and evaluation of an ultra-area-efficient fault-tolerant QCA full adder," *Microelectronics Journal*, Vol 46, No. 6, P. 531, 2015.

J7 **A. Roohi**[*], H. Khademolhosseini, S. Sayedsalehi, and K. Navi, ''A Symmetric Quantum-dot Cellular Automata Design for 5-input Majority Gate," *Journal of Computational Electronics*, Vol 13, No. 3, P. 701, 2014.

J6 **A. Roohi***, H. Khademolhosseini, ‘‘Quantum-Dot Cellular Automata: Computing in Nanoscale,” *Reviews In Theoretical Science (RITS)*, Vol 2, No. 1, P. 46, 2014.

J5 H. Shabani*, **A. Roohi***, A. Reza, H. Khademolhosseini, and M. Reshadi, ‘‘Parallel-XY: a novel loss-aware non-blocking photonic router for silicon nano-photonic networks-on-chip,” *Journal of Computational and Theoretical Nanoscience*, Vol.10, No.6, P. 1510, 2013.

J4 K. Navi*, **A. Roohi**, and S. Sayedsalehi, ‘‘Designing Reconfigurable Quantum-dot Cellular Automata Logic Circuits,” *Journal of Computational and Theoretical Nanoscience*, Vol.10, No.5, P. 1137, 2013.

J3 **A. Roohi**, S. Sayedsalehi, H. Khademolhosseini, and K. Navi*, ‘‘Design and Evaluation of a Reconfigurable Fault Tolerant Quantum-dot Cellular Automata Gate,” *Journal of Computational and Theoretical Nanoscience*, Vol.10, No.2, P. 380, 2013.

J2 S. Sayedsalehi, **A. Roohi**, and K. Navi*, ‘‘A different design approach for high performance in nanostructure using Quantum Cellular Automata,” *Canadian Journal on Electrical and Electronics Engineering*, Vol.2, No.11, P. 526, 2011.

J1 **A. Roohi**, H. Khademolhosseini, S. Sayedsalehi, and K. Navi*, ‘‘A Novel Architecture for Quantum-Dot Cellular Automata Multiplexer,” *International Journal of Computer Science Issues*, Vol.8, No.6, P. 55, 2011.

❑ Conference Papers

C54 N. Taheri, S. Tabrizchi, Sh. Angizi, and **A. Roohi***, “ChaoSen: Security Enhancement of Image Sensor through in-Sensor Chaotic Computing,” 42nd *IEEE International Conference on Computer Design (ICCD)*, Milan, Italy, 2024.

C53 R. Gaire, S. Tabrizchi, D. Najafi, Sh. Angizi, and **A. Roohi***, “DECO: Dynamic Energy-aware Compression and Optimization for In-Memory Neural Networks,” IEEE 67th *International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 11-14, 2024.

C52 R. Gaire, S. Tabrizchi, and **A. Roohi***, “Resource-Efficient Adaptive-Network Inference Framework with Knowledge Distillation-based Unified Learning,” *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Knoxville, Tennessee, USA, July 1-2, 2024.

C51 M. Morsali, R. Velpula, M. Muthu, H. Nguyen, M. Imani, **A. Roohi**, R. Zand, and Sh. Angizi*, “Energy-Efficient Near-Sensor Event Detector based on Multilevel Ga_2O_3 RRAM,” *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Knoxville, Tennessee, USA, July 1-2, 2024.

C50 N. Taheri, S. Tabrizchi, D. Najafi, Sh. Angizi, and **A. Roohi***, “ResSen: Imager Privacy Enhancement through Residue Arithmetic Processing in Sensors,” *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Knoxville, Tennessee, USA, July 1-2, 2024.

C49 D. Najafi, S. Tabrizchi, R. Zhou, M. Solouki, A. Marshal, **A. Roohi**, and Sh. Angizi*, “Hybrid Magneto-electric FET-CMOS Integrated Memory Design for Instant-on Computing,” ACM *Great Lakes Symposium on VLSI (GLSVLSI 2024)*, June 12-14, 2024.

C48 S. Tabrizchi, N. Taheri, Sh. Angizi, and **A. Roohi***, “RACSen: Residue Arithmetic and Chaotic Processing in Sensors to Enhance CMOS Imager Security,” ACM *Great Lakes Symposium on VLSI (GLSVLSI 2024)*, June 12-14, 2024.

C47 B. Reidy, S. Tabrizchi, M. Mohammadi, Sh. Angizi, **A. Roohi**, and R. Zand*, “HiRISE: High-Resolution Image Scaling for Edge ML via In-Sensor Compression and Selective ROI,” *61st Design Automation Conference (DAC)*, San Francisco, CA, USA, July 23-27, 2024.

C46 M. Morsali, B. Reidy, D. Najafi, S. Tabrizchi, M. Imani, M. Nikdast, **A. Roohi**, R. Zand, and Sh. Angizi*, “Lightator: An Optical Near-Sensor Accelerator with Compressive Acquisition Enabling Versatile Image Processing,” *61st Design Automation Conference (DAC)*, San Francisco, CA, USA, July 23-27, 2024.

C45 S. Tabrizchi, Sh. Angizi, and **A. Roohi***, “DIAC: Design Exploration of Intermittent-Aware Computing Realizing Batteryless Systems,” 44th *Design, Automation and Test in Europe Conference (DATE)*, Valencia, Spain, 25 - 27 March 2024.

C44 M. Morsali, S. Tabrizchi, D. Najafi, M. Imani, M. Nikdast, **A. Roohi**, Sh. Angizi*, "OISA: Architecting an Optical In-Sensor Accelerator for Efficient Visual Computing," 44th *Design, Automation and Test in Europe Conference (DATE)*, Valencia, Spain, 25 - 27 March 2024.

C43 R. Zhou, S. Ahmed, **A. Roohi**, A. Rakin, and Sh. Angizi*, "DRAM-Locker: A General-Purpose DRAM Protection Mechanism against Adversarial DNN Weight Attacks," 44th *Design, Automation and Test in Europe Conference (DATE)*, Valencia, Spain, 25 - 27 March 2024.

C42 M. Morsali, S. Tabrizchi, M. Liehr, N. Cady, M. Imani, **A. Roohi**, and Sh. Angizi*, "Deep Mapper: A Multi-Channel Single-Cycle Near-Sensor DNN Accelerator," IEEE *International Conference on Rebooting Computing (ICRC)*, December 5-6, 2023.

C41 R. Gaire, S. Tabrizchi, and **A. Roohi***, "EnCoDe: Enhancing Compressed Deep Learning Models through Feature Distillation and Informative Sample Selection," IEEE 22nd *International Conference on Machine Learning and Applications (ICMLA)*, December 15-17, 2023.

C40 S. Tabrizchi, Sh. Angizi, and **A. Roohi***, "Ocellus: Highly Parallel Convolution-in-Pixel Scheme Realizing Power-Delay-Efficient Edge Intelligence," ACM/IEEE *International Symposium on Low Power Electronics and Design (ISLPED)*, August 7-8, 2023. **(Best Paper Candidate)**

C39 D. Vungarala, M. Morsali, S. Tabrizchi, **A. Roohi**, and Sh. Angizi*, "Comparative Study of Low Bit-width DNN Accelerators: Opportunities and Challenges," IEEE 66th *International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 6-9, 2023.

C38 S. Tabrizchi, R. Gaire, Sh. Angizi, and **A. Roohi***, "SenTer: A Reconfigurable Processing-in-Sensor Architecture Enabling Efficient Ternary MLP," 33rd ACM *Great Lakes Symposium on VLSI (GLSVLSI 2023)*, June 5-7, 2023.

C37 S. Tabrizchi, M. Morsali, Sh. Angizi, and **A. Roohi***, "NeSe: Near-Sensor Event-Driven Scheme for Low Power Energy Harvesting Sensors," 24th IEEE *International Symposium on Circuits and Systems (ISCAS)*, Monterey, California, May 21-25, 2023.

C36 M. Morsali, R. Zhou, S. Tabrizchi, **A. Roohi***, and Sh. Angizi*, "XOR-CiM: An Efficient Computing-in-SOT-MRAM Design for Binary Neural Network Acceleration," 24th IEEE *International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, April 5-7, 2023.

C35 R. Zhou, S. Tabrizchi, **A. Roohi**, and Sh. Angizi*, "P-PIM: A Parallel Processing-in-DRAM Framework Enabling RowHammer Protection," 43rd *Design, Automation and Test in Europe Conference (DATE)*, Antwerp, BE, 2023.

C34 A. Minhaz, **A. Roohi***, N. Cady, and Sh. Angizi*, "A Processing-in-Pixel Accelerator based on Multi-level HfOx ReRAM," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (ESWEEK CASES)*, 2022.

C33 S. Tabrizchi, Sh. Angizi, and **A. Roohi***, "TizBin: A Low-Power Image Sensor with Event and Object Detection Using Efficient Processing-in-Pixel Schemes," 40th *IEEE International Conference on Computer Design (ICCD)*, Lake Tahoe, USA, 2022.

C32 R. Zhou, S. Tabrizchi, **A. Roohi***, and Sh. Angizi*, "ReD-LUT: Reconfigurable In-DRAM LUTs Enabling Massive Parallel Computation," 41st *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, California, USA, 2022.

C31 A. Nezhadi, Sh. Angizi, and **A. Roohi***, "semiMul: Floating-Point Free Implementations for Efficient and Accurate Neural Network Training," 21st *IEEE International Conference on Machine Learning and Applications (ICMLA)*, 2022.

C30 S. Tabrizchi, Sh. Angizi, and **A. Roohi***, "Design and Evaluation of a Robust Power-Efficient Ternary SRAM Cell," *IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1-4. IEEE, 2022.

C29 M. Alali, **A. Roohi**, J. S. Deogun*, "Enabling efficient training of convolutional neural networks for histopathology images," *International Conference on Image Analysis and Processing*, pp. 533-544. Springer, Cham, 2022.

C28 R. Zhou, **A. Roohi**, D. Misra, and Sh. Angizi*, "FlexiDRAM: A Flexible in-DRAM Framework to Enable Parallel General-Purpose Computation," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, Boston, USA, 2022.

C27 **A. Roohi***, and Sh. Angizi, "Efficient Targeted Bit-Flip Attack Against the Local Binary Pattern Network," *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, Washington DC, USA, 2022.

C26 S. Tabrizchi, Sh. Angizi, and **A. Roohi***, "SCiMA: a Generic Single-Cycle Compute-in-Memory Acceleration Scheme for Matrix Computations," 23rd IEEE *International Symposium on Circuits and Systems (ISCAS)*, Austin, TX, May 28- June 1, 2022.

C25 A. Nezhadi, Sh. Angizi, and **A. Roohi***, "EaseMiss: HW/SW Co-Optimization for Efficient Large Matrix-Matrix Multiply Operations," 15th IEEE *Dallas Circuit And System Conference (DCAS)*, pp. 1-6. IEEE, 2022.

C24 Sh. Angizi*, and **A. Roohi***, "Integrated Sensing and Computing using Energy-Efficient Magnetic Synapses," 23rd IEEE *International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, April 6-8, 2022.

C23 **A. Roohi***, Sh. Angizi, P. Navaeilavasani, and M. Taheri, "ReFACE: Efficient Design Methodology for Acceleration of Digital Filter Implementations," 23rd IEEE *International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, April 6-8, 2022.

C22 **A. Roohi***, M. Taheri, Sh. Angizi, D. Fan, "RNSiM: Efficient Deep Neural Network Accelerator Using Residue Number Systems," *40th International Conference On Computer-Aided Design (ICCAD)*, 2021, pp. 1-9

C21 Sh. Angizi*, **A. Roohi***, M. Taheri, D. Fan, "Processing-in-Memory Acceleration of MAC-based Applications Using Residue Number System: A Comparative Study," *31st ACM Great Lakes Symposium on VLSI (GLSVLSI 2021)*, June 22-25, 2021.

C20 N. Khoshavi, S. Sargolzaei, Y. Bi, **A. Roohi***, "Entropy-Based Modeling for Estimating Adversarial Bit-flip Attack Impact on Binarized Neural Network," *26th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan.18-21, 2021.

C19 **A. Roohi***, "Normally-Off Computing Design Methodology Using Spintronics: From Devices to Architectures," *International Green and Sustainable Computing Conference*, October 19-22, 2020

C18 N. Khoshavi*, C. Broyles, Y. Bi, **A. Roohi**, "Fiji-FIN: A Fault Injection Framework on Quantized Neural Network Inference Accelerator," *IEEE International Conference on Machine Learning and Applications (ICMLA)*, October 19-22, 2020.

C17 N. Khoshavi*, **A. Roohi**, Y. Bi, "Hardware-assisted Black-box Adversarial Attack Evaluation Framework on Binarized Neural Network," *41st IEEE Symposium on Security and Privacy*, Short Talks, URL: https://www.ieee-security.org/TC/SP2020/program-shorttalks.html, 2020.

C16 N. Khoshavi*, **A. Roohi***, C. Broyles, S. Sargolzaei, Y. Bi, D. Z. Pan, "SHIELDeNN: Online Accelerated Framework for Fault-Tolerant Deep Neural Network Architectures," *57th Design Automation Conference (DAC)*, San Francisco, CA, USA, July 19-23, 2020.

C15 N. Khoshavi*, **A. Roohi**, S. Sargolzaei, C. Broyles, and Y. Bi, "Entropy-Based Modeling for Estimating Soft Errors Impact on Binarized Neural Network Inference," *arXiv preprint arXiv:2004.05089* 2020.

C14 **A. Roohi***, and R. F. DeMara, "IRC: Cross-layer design exploration of Intermittent Robust Computation units for IoTs," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Miami, Florida, U.S.A., July 15-17, 2019.

C13 **A. Roohi***, Sh. Angizi, D. Fan, and R. F. DeMara, "Processing-In-Memory Acceleration of Convolutional Neural Networks for Energy-Efficiency, and Power-Intermittency Resilience," 20th IEEE *International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, March 6-7, 2019. **(Best Paper Candidate)**

C12 **A. Roohi***, R. Zand, and R. F. DeMara, "Logic-Encrypted Synthesis for Energy-Harvesting-Powered Spintronic-Embedded Datapath Design," *28th ACM Great Lakes Symposium on VLSI (GLSVLSI 2018)*, Chicago, Illinois, USA, May 23-25, 2018. **(Best Paper Candidate)**

C11 **A. Roohi***, R. Zand, and R. F. DeMara, "Synthesis of Normally-Off Boolean Circuits: An Evolutionary Optimization Approach Utilizing Spintronic Devices," The 19th *International Symposium on Quality Electronic Design*, Santa Clara, CA, USA, ISQED 2018. **(Best Paper Candidate)**

C10 R. F. DeMara*, **A. Roohi**, R. Zand, and S. D. Pyle, "Heterogeneous Technology Configurable Fabrics for Field Programmable Co-design of CMOS and Spin-based Devices," in Proceedings of *IEEE International Conference on Rebooting Computing (ICRC-2017)*, Washington, DC, USA, November 8 - 9, 2017.

C9 **A. Roohi***, L. Wang, S. Kose, and R. F. DeMara, "Secure Intermittent-Robust Computation for Energy Harvesting Device Security and Outage Resilience," The 14th *IEEE International Conference on Advanced and Trusted Computing*, San Francisco, CA, USA, ATC 2017.

C8 A.M.Chabi, **A. Roohi**, H. Khademolhosseini, Sh. Angizi, R. F. DeMara, and K. Navi*, "Cost-Efficient QCA Reversible Combinational Circuits Based on a New Reversible Gate," The 18th *CSI Symposium on Computer Architecture & Digital Systems*, Tehran, Iran, CADS 2015 **(Best Paper Candidate)**.

C7 R. A. Ashraf, A. Al-Zahrani, N. Khoshavi, R. Zand, S. Salehi, **A. Roohi**, M. Lin, and R. F. DeMara*, "Reactive Rejuvenation of CMOS Logic Paths using Self-Activating Voltage Domains," *IEEE International Symposium on Circuits and Systems*, Lisbon, Portugal, ISCAS 2015.

C6 **A. Roohi***, R. F. DeMara, and N. Khoshavi, "Dual Computational Layer Based Logic Design for QCA Circuits," 52nd *Design Automation Conference (DAC)*, Work-in-Progress Session, San Francisco, CA, USA, DAC-WIP 2015.

C5 S. Sayedsalehi*, and **A. Roohi**, "Modeling an Improved Modified Type in Metallic Quantum-dot Fixed Cell for Nano Structure Implementation," 23rd *Euromicro International Conference on Parallel, Distributed and Network-based* Processing, Turku, Finland, PDP 2015.

C4 S. Sayedsalehi*, **A. Roohi**, H. Khademolhosseini, and M. Kamrani, "Design of Nanoelectronic Circuits Using an Efficient Reversible Gate," 9th *International Nanotechnology Symposium*, Dresden, Germany, Nanofair 2012.

C3 **A. Roohi***, H. Khademolhosseini, S. Sayedsalehi, and K. Navi, ''Implementation of Reversible Logic Design in Nanoelectronics on Basis of Majority Gates," The 16th *CSI Symposium on Computer Architecture & Digital Systems*, Shiraz, Iran, CADS 2012.

C2 **A. Roohi***, M. Kamrani, S. Sayedsalehi, and K. Navi, ''A Combinational Logic Optimization for Majority Gate-Based Nanoelectronic Circuits Based on GA," *International Semiconductor Device Research Symposium*, The University of Maryland, USA, ISDRS 2011.

C1 H. Khademolhosseini and **A. Roohi***, ''A New Redundant Method on Representing Numbers with Moduli Set $\{3^n, 3^n - 1, 3^n - 2$ " *Computer, Communication and Electrical Technology (ICCCET 2011)*, IEEE International Conference on, pp. 163-166, 2011.

❑ Book Chapter

Ch3 **A. Roohi***, Sh. Angizi, and D. Fan, "Enabling Edge Computing Using Emerging Memory Technologies: From Device to Architecture," *In Frontiers of Quality Electronic Design (QED) AI, IoT and Hardware Security*, Cham: Springer International Publishing, pp. 415-464, 2022.

Ch2 R. Zand*, **A. Roohi***, and R. F. DeMara, "Fundamentals, Modeling, and Application of Magnetic Tunnel Junction," *Nanoscale Devices: Physics, Modeling, and Their Applications*, CRC Press, pp. 337-368, 2018.

Ch1 M. Kamrani*, H. Khademolhosseini, **A. Roohi**, and P. Aloustanimirmahalleh, ''A Novel Genetic Algorithm Based Method for Efficient QCA Circuit Design," *Advances in Computer Science, Engineering & Applications*. vol. 166, D. C. Wyld, et al., Eds., ed: Springer Berlin / Heidelberg, pp. 433-442, 2012.

❑ Patents

P2 Sh. Angizi and **A. Roohi**, *"A Non-Volatile Processing-In-Sensor Accelerator for Imaging Systems,"*, U.S. Patent Application 18/439,267.

P1 **A. Roohi**[*] and Sh. Angizi *"Convolution-in-Pixel Scheme for Neural Network Acceleration Enabling Edge Intelligence,"* Patent Pending.

Funding Experience

❑ Awarded at University of Nebraska Lincoln (UNL)

2024-2029 **National Science Foundation (NSF):**, *"CAREER: Elastic Intermittent Computation Enabling Batteryless Edge Intelligence"*, 8/1/2024 - 7/30/2029; Role: **Leading-PI**; total awarded fund: **$679,831**.
Abstract

2024-2026 **National Science Foundation (NSF): CSR: Small**, *"Cross-Layer Solutions Enabling Instant Computing for Edge Intelligence Devices"*, 1/1/2024 - 12/30/2026; Role: **Leading-PI**; total awarded fund: **$533,880**, UIC: $364,960.
Abstract

2023-2026 **National Science Foundation (NSF): SaTC: CORE: Medium**, *"Collaborative Research: Security and Robustness for Intermittent Computing Using Cross-Layer Post-CMOS Approaches"*, 10/1/2023 - 09/30/2026; Role: **Leading-PI**; total awarded fund: **$1.2M**, UIC: $399,972.
Abstract

2023-2025 **Grand Challenges Catalyst (UNL)**, *"Quantum Solutions for Energy Challenges: A Collaborative Leap towards Sustainability"*, 8/2023 - 07/2025; Role: **Co-PI**; total awarded fund: **$150,000**.

2022-2025 **National Science Foundation (NSF): CCSS**, *"Collaborative Research: Integrated Sensing and Normally-off Computing for Edge Imaging Systems"*, 10/1/2023 - 09/30/2026; Role: **Co-PI**; total awarded fund: **$539,998**, UNL: $260,664.
Abstract

2023-2024 **National Science Foundation (NSF): CSR**, *"Student Participation Grant for 2022 IEEE International Conference on Green and Sustainable Computing (IEEE IGSC)"*, Role: **Sole-PI**; total awarded fund: $10,000.
Abstract

2022-2023 **University of Nebraska-Lincoln: Layman Award**, *"Enabling Robust Quantized Neural Network Acceleration in Federated Edge Computing"*, Role: **Sole-PI**; total awarded fund: $10,000.

2021-2022 **National Science Foundation (NSF): CSR**, *"Student Participation Grant for 2021 IEEE International Conference on Green and Sustainable Computing (IEEE IGSC)"*, Role: **Sole-PI**; total awarded fund: $10,000.

❑ Awarded at University of Central Florida (UCF)

2018-2019 **Graduate Grantsmanship Series: 2018-2019**, learn to search for funding opportunities, plan research proposals and budgets, and manage sponsored research activities.

2017-2020 **NSF Energy-Efficient Computing: from Devices to Architectures (E2CDA) Collaborative Proposal**, Contributed to the UCF student contributions to prepare the proposal titled "Probabilistic Spin Logic for Low-Energy Boolean and Non-Boolean Computing", incl. 3-years REU Supplement: $2,501,754.

2017-2020 **Semiconductor Research Corporation (SRC)**, SRC Center: Probabilistic Spin Logic for Low-Energy Boolean and Non-Boolean Computing, an extra grant as a part of E2CDA: $1,226,877.

2016-2017 **The Florida Center for Cybersecurity (FC2) collaborative Proposal**, Leading the UCF student contributions to prepare the proposal titled "Trusted IoT using Cross-layer Leveraging of Reconfigurable Device Signatures", $25,000.

2015-2016 **The Florida Center for Cybersecurity (FC2) collaborative Proposal**, Contributed to the UCF student contributions to prepare the proposal titled "Aging-Aware Hardware-Trojan Detection at Runtime", $25,000.

Teaching Experience

❑ **University of Nebraska-Lincoln (UNL)**

2020-present **Instructor**, **CSCE 431/831: Hardware Acceleration for Machine Learning**, University of Nebraska - Lincoln

- Foundations of ML and DL algorithm
- Compute and memory behavior of DL workloads
- HW+ML for the compute-heavy deep neural network (DNN) models of machine learning
- Co-design of ML algorithms and accelerators

2021-present **Instructor**, **CSCE 430/830: Computer Architecture**, University of Nebraska - Lincoln

- Foundations of computer architecture
- Instruction set architecture
- Memory hierarchy, and cache design/optimization
- Pipelining and parallelism

2023-present **Instructor**, **CSCE 351: Operating System Kernels**, University of Nebraska - Lincoln

- Foundations of cache and virtual memory
- Process management (Scheduling)
- Process and thread synchronization
- Handling of interrupts and exceptions and system calls

❑ **University of Central Florida (UCF)**

2016-2018 **Tutor/Proctor/Coordinator**, Evaluation and Proficiency Center (EPC), University of Central Florida

- Played a pivotal role in the development of infrastructure, procedures, and online question content for secure quiz delivery interwoven with post-testing review.
- Lead assistant in 120-seat testing center to proctor computer-based examinations for Electrical and Computer Engineering undergraduate courses.
- Provided review-based tutoring for students.
- Developed high-quality electronically-delivered question content used in Electrical and Computer Engineering undergraduate courses.

2016-2017 **STEM Assessment Assistant:** Advisement of faculty at all levels (Lecturer through Professor) on digitization of engineering assessments, construction of computer-based exams, and remediation methods.

Sep 2015-Aug 2016 **Graduate Teaching Assistant**, Electrical and Computer Engineering, University of Central Florida

- Embedded Systems

Jan 2015-Aug 2015 **Graduate Assistant**, Electrical and Computer Engineering, University of Central Florida, Orlando, FL, USA.

Academic Services & Activities

2017-2019 Vice President of Students Laureates of STEM Teaching and Learning (SLSTL) Registered Student Organization.

2016-2017 Treasurer of Students Laureates of STEM Teaching and Learning (SLSTL) Registered Student Organization.

2016 Co-Established Students Laureates of STEM Teaching and Learning (SLSTL) as a Registered Student Organization.

❑ Memberships in Professional Organizations

2023-present AAAI Lifetime Member
2023-present IEEE Senior Member
2020-present ACM Lifetime Professional Member
2023-present IEEE Circuits and Systems Society
2020-present IEEE Systems Council Member
2020-present IEEE Computer Society Member
2020-present IEEE Council on Electronic Design Automation Member
2020-present ACM SIGARCH Member
2020-present ACM SIGMICROl Member
2020-present ACM SIGDA Member

❑ Editorial Board

2021-present Associate Editor of **Micromachines Journal.**
2019-present Associate Editor of **Neural Processing Letters.**
2014-present International Journal of VLSI Design & Communication Systems (**VLSICS**).
2014-2017 International Journal of Advanced Computer Research (**IJACR**).

❑ Technical Program Committees

2023 tinyML Research Symposium
2020-2022 IEEE/ACM Design Automation Conference (DAC)
2020-present Silicon Valley Cybersecurity Conference (SVCC)
2019-present IEEE Computer Society Annual Symposium on VLSI (ISVLSI)
2019-present ACM Great Lakes Symposium on VLSI (GLSVLSI)
2018-present IEEE International Symposium on Quality Electronic Design (ISQED)
2021-2022 IEEE International Conference on Computer Design (ICCD)
2021-2022 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)
2021-2023 International Conference on VLSI Design (VLSID)
2022 IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
2013 Second International Conference on Soft Computing, Artificial Intelligence and Applications.
2013 International Conference On Emerging Trends, Technology and Research.
2012 First International Conference on Emerging Trends and Technology.

❑ Leadership Positions in International and National Organizations

2023 Organized *"DAC Early Career,"* workshop, which was co-located with DAC
2023 Session Chair - tinyML Research Symposium (2023)
2020–2023 Session Chair - IEEE Computer Society Annual Symposium on VLSI (ISVLSI)
2020–2022 Session Chair - ACM Great Lakes Symposium on VLSI (GLSVLSI) Conference
2020–2022 Session Chair - IEEE/ACM Design Automation Conference (DAC)
2022 Session Chair - IEEE International Conference on Computer Design (ICCD)
2022 Session Chair - International VLSI Design & Embedded Systems Conference (VLSID)
2021–2022 Session Chair - IEEE International Symposium on Quality Electronic Design (ISQED)
2021–2022 Travel Grant Chair - IEEE International Green and Sustainable Computing Conference (IGSC)
2021 Organized *"Neuromorphic Computing: from Material to Algorithm (NeuMA),"* workshop, which was co-located with IGSC
2021 Ph.D. Forum Chair - IEEE International Green and Sustainable Computing Conference (IGSC)

❑ Technical Reviewer

- IEEE Transactions on Computers (TC)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Circuits and Systems I (TCAS I)
- IEEE Transactions on Circuits and Systems II (TCAS II)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Nanotechnology (TNANO)
- IEEE Transactions on Emerging Topics in Computing (TETC)
- IEEE Access
- IET Computers & Digital Techniques
- ACM Journal of Emerging Technologies in Computing Systems
- Journal of Computational Electronics (Springer)
- International Journal of Theoretical Physics (Springer)
- Microelectronics Journal (Elsevier)
- Microprocessors and Microsystems (Elsevier)
- AEU - International Journal of Electronics and Communications (Elsevier)
- Ain Shams Engineering Journal (Elsevier)
- International Journal of Electronics Letters(Taylor & Francis)
- IETE Journal of Research (Taylor & Francis)
- ETRI Journal (Wiley)
- Sub-reviewer for IEEE Asia and South Pacific Design Automation Conference (**ASP-DAC: 2020**)
- Sub-reviewer for IEEE Computer Society Annual Symposium on VLSI (**ISVLSI: 2016 - 2018**)
- International Conference on Semiconductor Devices, Circuits and Systems (**SDCS 2013)**
- IEEE International Conference on Technological Advances in Electrical, Electronics and Computer Engineering (**TAEECE 2013**).
- International Conference on Advance Computing & Communication (**ICACC 2013**).

Selected Invited Talks & Presentations

2023 **Edge Imaging Systems: The Role of Integrated Sensing and Intermittent Computing**, *National Science Foundation (NSF) Principal Investigator (PI) Meeting of the Computer Systems Research (CSR) Program.*

2023 **Edge Imaging Systems: The Role of Integrated Sensing and Normally-off Computing**, *Multicore and Multiprocessor SoCs (MPSoC).*

2023 **MR-PIPA: An Integrated Multilevel RRAM (HfOx)-Based Processing-In-Pixel Accelerator**, *Solid-State Circuits Society (SSCS) Open Journal Webinar Series.*

2020 **Normally-Off Computing Design Methodology Using Spintronics: From Devices to Architectures**, *Computing with Unconventional Technologies (CUT) Workshop, IGSC 2020.*

2020 **Enabling Efficient and Reliable Edge Computing: From Device to Architecture**, *Nebraska Center for Materials & Nanoscience, UNL.*

2019 **Processing In-Memory Architecture: from Non-Volatile Memories to Co-Processor Units**, *University of Texas at Austin, Austin, USA.*

2019 **Elastic Intermittent Computation for Energy-Harvesting-Powered Devices**, *Florida International University, Miami, USA.*

2019 **Elastic Intermittent Computation for Energy-Harvesting-Powered Devices**, *Mississippi State University, Mississippi, USA.*

2019 **Elastic Intermittent Computation for Energy-Harvesting-Powered Devices**, *University of Nevada, Reno, USA.*

2018 **Normally-Off Computing Design Methodology Using Spintronics: from Devices to Architectures**, *University of Central Florida, Orlando, USA*.

2018 **Intermittent Computation for Energy-Harvesting-Powered Devices Using Selectively Non-Volatile Datapaths**, *55th Design Automation Conference (DAC), San Francisco, CA, USA*.

2018 **Non-Volatile Logic-In-Memory Computation Using Spin-Hall-Effect-Based Datapaths**, *University of Central Florida, Orlando, USA*.

2016 **Review of Spintronics and functionalities of circuit based on Spin Hall Effect MTJ**, *University of Central Florida, Orlando, USA*.

2016 **Spin-Based Neuron Model With Domain-Wall Magnets as Synapse, Tehran, Iran**, *University of Central Florida, Orlando, USA*.

2015 **Domain Wall LFSR: a Novel Spintronic Circuit for Generating Weakly-Chaotic Signatures**, *University of Central Florida, Orlando, USA*.